

IN THE CLAIMS:

Please note that all of the claims that remain pending and under consideration in the above-referenced application are shown below, in clean form, for clarity. A marked-up version of each amended claim is also enclosed herewith to clearly identify the changes that have been made to each such claim.

Please cancel claims 88-101 without prejudice or disclaimer.

Please enter the claims as follows:

1. (Amended) A method for disposing a material on a semiconductor device structure, comprising:
providing a semiconductor device structure including a surface and at least one recess formed in said surface;
disposing said material on said surface so as to substantially fill said at least one recess, said material covering said surface having a thickness less than a depth of said at least one recess without subsequently removing said material from over said surface.

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2. (Amended) The method of claim 1, wherein said disposing comprises disposing said material so as to substantially fill said at least one recess without substantially covering said surface.

3. (Amended) The method of claim 1, wherein said disposing comprises:
applying said material to said surface of said semiconductor device structure;
spinning said semiconductor device structure;
decreasing a rate of said spinning while permitting said material to at least partially cure; and
gradually increasing said rate of said spinning.

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4. (Amended) The method of claim 3, further comprising exposing said material to a soft baking temperature following said gradually increasing.

5. The method of claim 3, wherein said spinning is effected at a rate of about 1,000 rpm.

6. The method of claim 3, wherein said decreasing said rate comprises decreasing said rate of said spinning to about 100 rpm.

7. The method of claim 3, wherein said gradually increasing said rate comprises gradually increasing said rate of said spinning to at least about 1,000 rpm.

8. (Amended) The method of claim 1, wherein, upon exposing said material disposed over an entirety of said semiconductor device structure to an etchant, said material covering said surface is substantially removed therefrom, while said material located in said at least one recess substantially fills said at least one recess.

9. The method of claim 1, wherein said providing said semiconductor device structure comprises providing a stacked capacitor structure with said at least one recess comprising at least one container formed in an insulator layer of said stacked capacitor structure, said surface and said at least one container being lined with a conductive material.

10. The method of claim 9, wherein said providing said semiconductor device structure comprises providing said stacked capacitor structure with said surface and said at least one container being lined with doped hemispherical grain polysilicon.

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11. (Amended) The method of claim 9, wherein said disposing said material comprises disposing a mask material over said semiconductor device structure.

12. The method of claim 1, wherein said providing said semiconductor device structure comprises providing a shallow trench isolation structure with said at least one recess comprising at least one trench formed in a surface of said shallow trench isolation structure.

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13. (Twice amended) The method of claim 12, wherein said disposing said material comprises disposing a mask material over said shallow trench isolation structure.

14. (Previously Amended) The method of claim 12, wherein said providing said shallow trench isolation structure comprises providing said shallow trench isolation structure with an insulator layer substantially filling said at least one trench and covering said surface.

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15. (Amended) The method of claim 14, wherein said disposing said material comprises disposing a stress buffer over said insulator layer, said stress buffer having a substantially planar surface without removing material thereof following said disposing.

16. The method of claim 1, wherein said providing comprises providing a semiconductor device structure having a surface with at least one dual damascene trench recessed therein and a layer of conductive material with a nonplanar surface disposed in said at least one dual damascene trench and at least partially covering said surface.

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17. (Amended) The method of claim 16, wherein said disposing said material comprises disposing a stress buffer over said layer of conductive material, said stress buffer having a substantially planar surface without removing material thereof following said disposing.